CLAIMS:

What is claimed is:

1. A data and communication apparatus communicatively coupled with a multi-processor shared memory multimedia chip system for providing interprocessor communication while enhancing performance of each processor integral with said multi-processor shared memory multimedia chip system, said data and communication apparatus comprising:

a data memory to retrievably store data;

an instruction memory coupled with said data memory to retrievably store instructions;

an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data; and

an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said each processor to communicate with other processors disposed within said system.

2. The data and communication apparatus of Claim 1 further comprising:

multiple registers coupled with said data and communication apparatus, said registers adapted to provide enhanced configurability and control of said data and communication apparatus, said registers further

adapted to provide addressable memory storage locations for said retrievably stored data and said retrievable stored instructions, said registers separate from and in addition to the registers within said multi-processor shared memory multimedia chip system.

3. The data and communication apparatus of Claim 1 wherein said data and communication apparatus is coupled with said multi-processor shared memory multimedia chip system, wherein access to said data and communication apparatus is via an I/O space (bus), said I/O space (bus) separate from a memory space (bus) of said device, said I/O space pre-existent within said system.

4. The data and communication apparatus of Claim 1 wherein said data said retrievably stored in said data memory is an interrupt service routine, wherein access to retrieve said interrupt service routine is via said I/O space, such that traffic on said memory space is commensurately reduced, so as to ensure the time required to complete said interrupt service routine.

5. The data and communication apparatus of Claim 1 wherein said data said retrievably stored in said data memory unit is real-time kernel thread context data, wherein said access to retrieve said real-time kernel thread context data is via said I/O space, such that traffic on said memory space in commensurately reduced, so as to increase speed with which thread context switching is achieved.

6. The data and communication apparatus of Claim 1 wherein said instructions said retrievably stored in said instruction memory are a function of a particular process, said function having certain tendencies relative to said particular process, wherein after said particular process is completed, said function of said particular process is removed, such that a subsequent function of a subsequent process is then stored in said instruction memory unit.

7. The data and communication apparatus of Claim 1 wherein said incoming buffer is configured as a prefetch mechanism for a particular type of data, so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular type of data is reduced.

8. The data and communication apparatus of Claim 1 wherein said outgoing buffer enables said a processor of said multi-processor multimedia chip system to send said communications to other processors disposed within said multi-processor multimedia chip system while independently processing other tasks, such that said processing of said other tasks is not disrupted.

9. The data and communication apparatus of Claim 1 wherein said outgoing buffer monitors the number of active communications within said system, such that a maximum number of active communications is not

exceeded, so as to allow additional active communications to be placed within said system when said allowance will not exceed said maximum number.

10. A multi-processor shared memory multimedia chip system having a data and communication apparatus coupled with said multi-processor shared memory multimedia chip system, said data and communication apparatus for providing interprocessor communication while enhancing the performance of each processor within said multi-processor shared memory multimedia chip system, said data and communication apparatus comprising:

a data memory to retrievably store data;

an instruction memory coupled with said data memory to retrievable store instructions;

an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data; and

an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables a processor of said multi-processor multimedia chip system to communicate with other processors of said multi-processor shared memory multimedia chip system.

11. The multi-processor shared memory multimedia chip system of Claim 10 wherein said data and communication apparatus is further comprising:

multiple registers coupled with said data and communication apparatus, said registers for providing enhanced configurability and control of said data and communication apparatus, said registers separate from and in addition to the registers of said multi-processor shared memory multimedia chip system, said registers of said data and communication apparatus to provide addressable memory storage locations for said retrievably stored data and said retrievable stored instructions.

12. The multi-processor shared memory multimedia chip system of Claim 10 wherein said data and communication apparatus is coupled with said system, wherein said data and communication apparatus is accessible via an I/O space (bus), said I/O space pre-existent within said system, said I/O space (bus) separate from a memory space (bus) of said system.

13. The multi-processor shared memory multimedia chip system of Claim 10 wherein said data said retrievably stored in said data memory is an interrupt service routine, said interrupt service routine accessible via said I/O space so as to commensurately reduce traffic on said memory space (bus), such that the time required to complete said ISR is ensured.

14. The multi-processor shared memory multimedia chip system of Claim 10 wherein said data said retrievably stored in said data memory is

real-time kernel thread context (streaming) data, said real-time kernel thread context data accessible via said I/O space so as to commensurately reduce traffic on said memory space (bus), such that the time required to achieve real-time thread context switching is reduced.

15. The multi-processor shared memory multimedia chip system of Claim 10 wherein said instructions said retrievably stored in said instruction memory are a function of a particular process, said function having certain tendencies relative to said particular process, wherein after said particular process is completed, said function of said particular process is deleted, such that a subsequent function of a subsequent particular process is stored in said instruction memory.

16, The multi-processor shared memory multimedia chip system of Claim 10 wherein said incoming buffer is configured as a prefetch mechanism for a particular data type and enables acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular data type is reduced.

17. The multi-processor shared memory multimedia chip system of Claim 10 wherein said outgoing buffer enables a said processor of said multi-processor multimedia chip system to send said communications to other processors disposed within said system while simultaneously processing other tasks, such that said processing of other tasks is not disrupted.

18. The multi-processor shared memory multimedia chip system of Claim 10 wherein said outgoing buffer monitors the number of active communications within said system, such that a maximum number of active communications is not exceeded, so as to allow additional active communications to be placed within said system when said allowance will not exceed said maximum number.

19. In a multi-processor shared memory multimedia chip system having a memory space (bus) and an I/O space (bus), a method to provide interprocessor communication while enhancing processor performance, said method comprising the step of:

providing an data and communication apparatus adapted to be communicatively coupled to said multi-processor shared memory multimedia chip system, wherein access to said data and communication apparatus is via said I/O space, said data and communication apparatus further adapted to enable said interprocessor communication and said enhanced processor performance.

20. The method of Claim 19 further comprising the step of providing a data memory to retrievably store data.

21. The method of Claim 20 wherein said data said retrievably stored in said data memory is an interrupt service routine, said interrupt service routine accessible via said I/O space, such that traffic on said memory

space (bus) of said multi-processor shared memory multimedia chip system is commensurately reduced, so as to ensure the time required to complete said interrupt service routine.

22. The method of Claim 20 wherein said data said retrievably stored in said data memory is real-time kernel thread context (streaming) data, said real-time kernel thread context (streaming) data accessible via said I/O space, such that traffic on said memory space is commensurately reduced, so as to increase speed with which real-time thread context (streaming) data is switched.

23. The method of Claim 19 further comprising the step of providing an instruction memory coupled with said data memory to retrievably store instructions.

24. The method of Claim 23 wherein said instructions said retrievably stored in said instruction memory are a function of a particular process, said function having certain tendencies relative to said particular process, wherein following completion of said particular process, said function is deleted, such that a subsequent function of a subsequent process is then stored in said instruction memory.

24. The method of Claim 19 further comprising the step of providing an incoming buffer coupled with said data memory and said instruction memory, said incoming buffer adapted as a prefetch mechanism for a

particular data type, so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular data type is reduced.

25. The method of Claim 19 further comprising the step of providing an outgoing buffer coupled with said data memoryand said instruction memory, said outgoing buffer enables a processor of said multi-processor shared memory multimedia chip system to communicate with other processors disposed within said system while simultaneously processing other tasks, such that said processing of said other tasks in not disturbed.

26. The method of Claim 25 wherein said outgoing buffer monitors the number of active communications within said system, said system having a maximum number of active communications, so as to allow additional active communications to be placed within said system when said allowance will not exceed said maximum number.

27 The method of Claim 19 further comprising the step of providing multiple registers coupled with said data and communication apparatus, said registers adapted to provide enhanced configurability and control of said data and communication apparatus, said registers further adapted to provide addressable memory storage locations for said retrievably stored data and said retrievably stored instructions, said registers coupled with said data and

communication apparatus separate from and in addition to the registers of said multi-processor shared memory multimedia chip system.